OIPE IAP44 FEB 26 2007 PATENT & TRADEMARK OFFICE

PATENT
Docket No. 492322016900

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Akira Suzuki, Takashi Noma, Hiroyuki Shinogi, Yukihiro Takao, and Shinzo Ishibe

Serial No.: 10/784,888
Filing Date: Feburuary24,2004

For: MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

Examiner: SMITH,BRADLEY

Group Art Unit: 2891

# DECLARATION OF NORIKO KOMORIYA

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Noriko Komoriya declares under penalty of perjury under the laws of the United States of America as follows:

1. I am a citizen of Japan currently employed at Suto International Patent Office in Ota-shi, Gunma-ken, Japan. I have a good command both in English and Japanese languages.

2. I have translated Japanese Patent Application No.2003-046755, and the translation is a literal translation of the Japanese patent application.

I declare under penalty of perjury under the laws of the United Stares that the foregoing is true and correct. Executed at Ota-shi, Gunma-ken, Japan, this 23rd day of February, 2007.

N. Komoriya

Noriko Komoriya

[Document Name] Patent Application
[Reference No.] KAA1030007
[Filing Date] February 25, 2003
[Application to] Commissioner of Japan Patent Office
[International Patent Classification] H01L 23/12
[Inventor]
[Address or Current Address] c/o Sanyo Electric Co., Ltd., 2-5-5, Keihanhondori, Moriguchi-City, Osaka 570-8677 Japan
[Name] Akira Suzuki
[Inventor]
[Address or Current Address] c/o Sanyo Electric Co., Ltd., 2-5-5, Keihanhondori, Moriguchi-City, Osaka 570-8677 Japan
[Name] Takashi Noma
[Inventor]
[Address or Current Address] c/o Sanyo Electric Co., Ltd., 2-5-5, Keihanhondori, Moriguchi-City, Osaka 570-8677 Japan
[Name] Hiroyuki Shinogi
[ Inventor]
[Address or Current Address] c/o Sanyo Electric Co., Ltd., 2-5-5, Keihanhondori, Moriguchi-City, Osaka 570-8677 Japan
[Name] Yukihiro Takao
[Inventor]
[Address or Current Address] c/o Sanyo Electric Co., Ltd., 2-5-5, Keihanhondori, Moriguchi-City, Osaka 570-8677 Japan
[Name] Shinzo Ishibe
[Applicant]
[Identification No.] 000001889
[Name or Company's Name] Sanyo Electric Co., Ltd.
[Representative] Yukinori Kuwano
[Agent]
[Identification No.] 100111383
[Attorney]
[Name] Tadamasa Shibano
[Contact] 03-3837-7751, Intellectual Property Rights department, Tokyo Office
[Fee]
[No. of Pre-payment] 013033
[Amount of Payment] ¥ 21,000

[Filing Objects]

[Object] Specification 1

[Object] Drawing 1

[Object] Abstract 1

[No. of General Power of Attorney] 9904451

[Proof] Yes

[Document Name] Specification

[Title of the Invention] MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

[Claims]

[Claim 1] A manufacturing method of a semiconductor device comprising:

bonding a supporting substrate with an adhesive to a surface of a semiconductor wafer on which a semiconductor element is formed;

grinding a surface of the semiconductor wafer which is opposite to the surface of the semiconductor wafer to which the supporting substrate is bonded with a back-grinder; and

reducing roughness of the back-ground surface of the semiconductor wafer by wet-etching to smooth the surface.

[Claim 2] A manufacturing method of a semiconductor device comprising:

bonding a supporting substrate with an adhesive to a surface of a semiconductor wafer on which a semiconductor element is formed;

forming a groove in the semiconductor wafer by etching a surface of the semiconductor wafer which is opposite to the surface of the semiconductor wafer to which the supporting substrate is bonded; and

rounding a corner of the groove by wet-etching the etched surface of the semiconductor wafer.

[Claim 3] The manufacturing method of the semiconductor device of claim 1 or 2, wherein the wet-etching is made by dropping chemical solution on the semiconductor wafer while holding the back-ground surface and the etched surface upward and spinning the semiconductor wafer to spread the chemical solution over whole area of the semiconductor wafer.

[Claim 4] The manufacturing method of the semiconductor device of claim 1, 2 or 3, wherein the wet-etching is made by dropping chemical solution on the semiconductor wafer while holding the back-ground surface and the etched surface upward, spinning the semiconductor wafer to spread the chemical solution over whole area of the semiconductor wafer, and a direction of rotation of the spinning is reversed.

[Claim 5] The manufacturing method of the semiconductor device of claim 1, wherein the wet-etching is made by grinding the back-ground surface with a CMP apparatus for reducing roughness of the surface and smoothing the surface.

[Claim 6] The manufacturing method of the semiconductor device of claim 1, 2, 3, 4, or 5 wherein the wet-etching or the grinding with the CMP apparatus is made to remove a foreign

particle on the back-ground surface and the etched surface.

[Claim 7] A manufacturing method of a semiconductor device comprising:

forming a pair of first wirings on a surface of a semiconductor wafer through an insulation film, the pair of first wirings facing each other across a border between neighboring semiconductor elements formed in the semiconductor wafer;

bonding a supporting substrate through an adhesive so that the pair of first wirings is covered with the supporting substrate;

back-grinding a surface of the semiconductor wafer which is opposite to the surface of the semiconductor wafer to which the supporting substrate is bonded; and

reducing roughness of the back-ground surface of the semiconductor wafer by wet-etching the back-ground surface.

[Claim 8] A manufacturing method of a semiconductor device comprising:

forming a pair of first wirings on a surface of a semiconductor wafer through an insulation film, the pair of first wirings facing each other across a border between neighboring semiconductor elements formed in the semiconductor wafer;

bonding a supporting substrate through an adhesive so that the pair of first wirings is covered with the supporting substrate;

back-grinding a surface of the semiconductor wafer which is opposite to the surface of the semiconductor wafer to which the supporting substrate is bonded;

reducing roughness of the back-ground surface of the semiconductor wafer by wet-etching the back-ground surface;

patterning a photoresist film disposed on the back-ground surface of the semiconductor wafer and etching the semiconductor wafer using the photoresist film as a mask to form a groove in the semiconductor wafer along the border between the semiconductor elements; and

wet-etching the etched surface of the semiconductor wafer including the groove to round a corner of the groove.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

This invention relates to a BGA (Ball Grid Array) type semiconductor device with ball-shaped conductive terminals.

[0002]

[Background Art]

The CSP (Chip Size Package) receives attention in recent years as a three-dimensional mounting technology as well as a new packaging technology. The CSP means a small package having about the same outside dimensions as those of a semiconductor die.

[0003]

A BGA type semiconductor device has been known as a kind of CSP. A plurality of ball-shaped conductive terminals made of metal such as solder is arrayed in a grid pattern on one principal surface of a package of the BGA type semiconductor device and is electrically connected with the semiconductor die mounted on the other side of the package.

[0004]

When the BGA type semiconductor device is mounted into electronic equipment, the semiconductor die is electrically connected with an external circuit on a printed circuit board by compression bonding of each of the conductive terminals to each of wiring patterns on the printed circuit board.

[0005]

Such a BGA type semiconductor device has advantages in providing a large number of conductive terminals and in size reduction over other CSP type semiconductor devices such as an SOP (Small Outline Package) and a QFP (Quad Flat Package), which have lead pins protruding from their sides. The BGA type semiconductor device is used as an image sensor chip for a digital camera incorporated into a mobile telephone, for example.

[0006]

Fig. 9 shows outline structure of a conventional BGA type semiconductor device. Fig. 9(A) is an oblique perspective figure showing a top side of the BGA type semiconductor device. And Fig. 9(B) is an oblique perspective figure showing a back side of the BGA type semiconductor device.

[0007]

A semiconductor die 101 is sealed between a first glass substrate 104a and a second glass substrate 104b through epoxy resins 105a and 105b in the BGA type semiconductor device 100. A plurality of ball-shaped terminals (hereafter referred to as conductive terminals 111) is arrayed in a grid pattern on a principal surface of the second glass substrate 104b, that is, on a back surface of the BGA type semiconductor device 100. The conductive terminals 111 are

connected to the semiconductor die 101 through a plurality of second wirings 109. The plurality of second wirings 109 is connected with metal wirings pulled out from inside of the semiconductor die 101, making each of the conductive terminals 111 electrically connected with the semiconductor die 101.

[0008]

More detailed explanation on a cross-sectional structure of the BGA type semiconductor device 100 will be given hereafter referring to Fig. 10. Fig. 10 shows a cross-sectional view of the BGA type semiconductor devices 100 divided along dicing lines into individual dice.

[0009]

The first wiring 103 is provided on an insulation film 102 on a top surface of the semiconductor die 101. The semiconductor die 101 is bonded to the first glass substrate 104a with the resin 105a. A back surface of the semiconductor die 101 is bonded to the second glass substrate 104b with the resin 105b. One end of the first wiring 103 is connected to the second wiring 109. The second wiring 109 extends from the end of the first wiring 103 to a surface of the second glass substrate 104b. The ball-shaped conductive terminal 111 is formed on the second wiring 109 extended onto the second glass substrate 104b.

[0010]

The above-described technology is described in the following patent document 1, for example.

[0011]

[Patent Document 1]

Japanese Patent Application Publication No. 2002-512436.

[0012]

[Problem to be solved by the Invention]

The glass substrates are bonded to both surfaces of the semiconductor die 101 in the BGA type semiconductor device 100 described above. However, it is not necessarily required that the second glass substrate 104b is bonded to the surface on which no semiconductor element is formed, in other words, the surface over which the conductive terminals are disposed. That is to say, there is no need for bonding the second glass substrate as long as the second wiring 109 is insulated from the semiconductor die 101. Thickness of the two glass substrates also makes up most of total thickness of the semiconductor device 100. Thus it is conceived that the glass substrate is bonded only to the surface of the semiconductor die 101 on which a semiconductor element is formed, so that cost and size of the semiconductor device 100 are reduced. An example of such a semiconductor device will be described using Fig. 8 which is a cross-sectional view of the semiconductor device according to this invention. The semiconductor device equivalent to the semiconductor device 100 is made by forming an insulation film 7 on the semiconductor die 1 instead of bonding the second glass substrate, and forming a cushioning pad

8, a second wiring 9, a protection film 10 and a conductive terminal 11 over the insulation film 7. However, there are problems to be described bellow in making such semiconductor device.

[0013]

(1) In manufacturing the BGA type semiconductor device, the surface opposite to the surface to which a glass substrate 4 is bonded, that is, a back surface of the semiconductor device is ground by back-grinding, prior to forming the insulation film 7. A semiconductor wafer is ground with a whetstone in the back-grinding for thinning. The back-grinding transfers bumps and dips on the whetstone to the surface of the wafer and causes scratches extending several microns in depth and length. The back-grinding scarcely causes a problem in the case of the semiconductor device 100 shown in Fig. 10, since the bumps and dips on the surface of the wafer due to the scratches are covered by the resin 105b and the glass substrates are bonded on both the sides.

[0014]

However, in the case of the BGA type semiconductor device having the glass substrate only on the surface on which the semiconductor element is formed, like in the case of the semiconductor device of this invention, it is required that an insulation film 7 is formed on the back-ground surface of the wafer in order to provide insulation between the die and the second wiring. Because the insulation film 7 is formed with a plasma CVD (Chemical Vapor Deposition) apparatus, the bumps and dips on the surface of the wafer are transferred to the insulation film 7 and the surface of the insulation film 7 is formed uneven. This causes poor coverage of photoresist films used in patterning the insulation film 7 and the second wiring 9. The poor coverage of the insulation film 7 may cause pinholes or cracks, making a contributing factor to deteriorate yield and reliability of the semiconductor device.

[0015]

(2) After the back-grinding, tapered grooves are formed by etching the semiconductor wafer along border lines of the semiconductor elements in order to divide the semiconductor elements into individual semiconductor dice. Residues and foreign particles attached to the etched surface of the semiconductor wafer cause bumps and dips on the surface of the semiconductor wafer. Also sharp edges are left at corners of the grooves after the etching. As a result, coverage of photoresist films for patterning, the second wiring 9 and the protection film 10 to be formed after forming the grooves is degraded, making additional factors to deteriorate yield and reliability of the semiconductor device.

[0016]

[Means for solving the Pr oblems]

This invention is directed to solve the problems addressed above, and offers a method to resolve the problems due to the bumps and dips on the surface of the back-ground semiconductor wafer, the bumps and dips on the surface of the etched semiconductor wafer and the sharp edges

at the corners left after forming the grooves by etching.

[0017]

According to this invention, wet-etching is applied to the semiconductor wafer after the back-grinding or the etching so that the bumps and dips on the wafer are smoothed and the sharp edges are rounded. With this, coverage of the photoresist films, the second wiring, the insulation film and the protection film formed after the back-grinding or the etching is improved, resulting in enhanced yield and reliability of the semiconductor device.

[0018]

[Description of the Invention]

A manufacturing method of a semiconductor device according to an embodiment of this invention will be described referring to Figs. 1 through 8.

[0019]

Refer to Fig. 1: A semiconductor wafer 1a, which will make semiconductor dice 1 in later process steps, is provided. The semiconductor dice 1 are CCD image sensor chips, for example, and are manufactured by semiconductor wafer processing. A pair of first wirings 3 separated by a predetermined spacing is formed on a surface of the semiconductor wafer through an insulation film 2 around a border (referred to as a dicing line or a scribe line) S to divide the wafer 1a into individual semiconductor dice 1. Each of the pair of first wirings 3 makes a pad extended from a bonding pad in the semiconductor die 1 to proximity of the border S. That is, each of the pair of first wirings 3 is a pad for external connection, and is electrically connected with a circuit in the semiconductor die 1, which is not shown in the figure.

[0020]

Then a supporting plate is bonded through an adhesive to the surface of the semiconductor wafer 1a on which the first wirings 3 are formed. A transparent epoxy resin 5 is used as the adhesive and a transparent glass substrate 4 is used as the supporting plate in the embodiment. When the BGA type semiconductor device of this invention is manufactured to house an LSI such as a memory or a microcomputer and does not house the CCD, an opaque plastic supporting plate may be bonded using a suitable adhesive.

[0021]

Refer to Fig. 2: A surface of the semiconductor wafer 1a opposite to the surface to which the glass substrate 4 is bonded is back-ground to reduce a thickness of the wafer. The thickness of the back-ground wafer is about 230 μm.

[0022]

On the back-ground surface of the semiconductor wafer 1a, scratches are caused to produce bumps and dips extending several microns in width and depth, as shown in an encircled portion (a: a surface before etching) in Fig. 2. The semiconductor wafer 1a is wet-etched using a chemical solution having high selection ratio between silicon (hereafter referred to as Si) which

is a material forming the semiconductor wafer 1a and a silicon oxide film (hereafter referred to as $SiO_2$) which is a material forming the glass substrate 4. The semiconductor wafer 1a is reduced in thickness by 5 to 30 μm by the wet-etching to obtain a surface with reduced bumps and dips, as shown in an encircled portion (b: a surface after etching) in Fig. 2.

[0023]

There is no specific restriction on the chemical solution used in the wet-etching, as long as it has high selection ratio between Si and $SiO_2$ as described above For example, a mixed solution composed of 2.5% of hydrofluoric acid, 50% of nitric acid, 10% of acetic acid and 37.5% of water is used as the silicon etching solution in this embodiment.

[0024]

Either of methods described below may be used as the wet-etching method.

[0025]

(1) A method is to reduce the roughness of the surface by wet-etching which includes dripping the chemical solution on the semiconductor wafer while holding the back-ground surface of the semiconductor wafer upward as in photoresist coating and spreading the chemical solution all over the semiconductor wafer by spinning the semiconductor wafer.

[0026]

In this method, the roughness on the surface is further reduced by reversing direction of rotation of the semiconductor wafer 1a to spread the chemical solution more equally all over the surface of the semiconductor wafer.

[0027]

(2) A method is to reduce the roughness on the surface by wet-etching performed by dipping the semiconductor wafer into the chemical solution.

[0028]

(3) A method is to reduce the roughness on the back-ground surface of the semiconductor wafer by CMP (Chemical Mechanical Polishing).

[0029]

Refer to Fig. 3: A photoresist film (not shown in the figure) which has an opening along the border S is formed on the surface of the semiconductor dies 1 opposite to the surface to which the glass substrate 4 is bonded. Isotropic etching using the photoresist film as a mask forms a tapered groove along the border S to expose the insulation film 2.

[0030]

Note that the isotropic etching may be done by either dry-etching or wet-etching.

[0031]

Bumps and dips as well as residues and foreign particles from the etching are left on the surface of the semiconductor wafer 1a after forming the groove. In addition, the semiconductor dice have sharp edges at corners of the tapered groove as shown in circles denoted a and b in Fig.

3.

[0032]

Refer to Fig. 4: Wet-etching is made to reduce the residues and the foreign particles and round the sharp edges. The sharp edges shown in encircled portions a and b in Fig. 3 are rounded off as shown in encircled portions a and b in Fig. 4.

[0033]

Chemical solution similar to one used in the wet-etching after the back-grinding may be used in the wet-etching. Following methods are applicable to the wet-etching.

[0034]

(1) A method of wet-etching after forming the groove is dripping the chemical solution on the semiconductor wafer 1a while holding the surface with the groove upward and spreading the chemical solution all over the semiconductor wafer 1a by spinning the semiconductor wafer.

[0035]

In this method, uniformity of the etching over the surface of the semiconductor wafer is improved since the chemical solution spreads more equally all over the semiconductor wafer 1a by reversing direction of rotation of the semiconductor wafer.

[0036]

(2) A method of the wet-etching after forming the groove is dipping the semiconductor wafer 1a into the chemical solution.

[0037]

Refer to Fig. 5: The insulation film 7 is formed on the surface of the semiconductor die 1 opposite to the surface to which the glass substrate 4 is bonded. A silane-based oxide film of 3 μm in thickness is formed in the embodiment.

[0038]

Refer to Fig. 6: A photoresist film (not shown) is applied on the surface opposite to the surface to which the glass substrate 4 is bonded and patterning is made to expose a portion of a bottom surface of each of the first wirings 3 in the semiconductor die 1. The insulation film 7 and the insulation film 2 are etched off using the photoresist film as a mask to expose the portion of the bottom surface of each of the first wirings 3. Next, flexible cushioning pads 8 are formed at locations above which the conductive terminals 11 are to be formed. The cushioning pads 8 have function to absorb power applied through the conductive terminals 11 and relax stress when the conductive terminals 11 are bonded. However this invention does not necessarily require including the cushioning pads 8.

[0039]

Then the second wiring 9 is formed on the surface opposite to the surface to which the glass substrate 4 is bonded. With this, the first wirings 3 are electrically connected with the

second wiring 9.

[0040]

Refer to Fig. 7: A photoresist film (not shown) is applied on the surface opposite to the surface to which the glass substrate 4 is bonded and pattering is made to form an opening in the photoresist film along the border S. Etching is done using the photoresist film as a mask to remove a portion of the second wiring 9 around the border S. After patterning the second wiring 9, electroless plating is made on the surface opposite to the surface to which the glass substrate 4 is bonded so that Ni-Au plating (not shown) is applied on the second wirings 9.

[0041]

Then the protection film 10 is formed on the surface opposite to the surface to which the glass substrate 4 is bonded. In order to form the protection film 10, the surface opposite to the surface to which the glass substrate 4 is bonded is held upward, a thermosetting organic resin is dropped on it and the organic resin is spread over the surface by spinning the semiconductor wafer 1a utilizing centrifugal force. With this, the protection film 10 is formed on a surface of the second wirings 9.

[0042]

Refer to Fig. 8: Portions of the protection film 10 at locations where the conductive terminals 11 are to be formed and around the border S are removed by etching using a photoresist film as a mask. Then the conductive terminals 11 are formed in these portions. Finally, the wafer is cut along the border S to complete the BGA type semiconductor device.

[0043]

[Effect of the Invention]

With this invention, the problems in manufacturing the thin BGA type semiconductor device are solved and yield and reliability of the BGA type semiconductor device are improved. The contents are as follows.

[0044]

(1) After a supporting plate is bonded to a surface of a semiconductor wafer formed with a plurality of semiconductor elements and a surface opposite to the surface to which the supporting plate is bonded is back-ground, the back-ground surface of the semiconductor wafer with bumps and dips extending several microns in width and depth due to scratches is wet-etched to reduce its roughness and enhance the coverage of films.

[0045]

(2) Wet-etching is performed to the semiconductor wafer with bumps and dips caused by residues and foreign particles and sharp edges which are caused by etching for forming tapered grooves along die border lines after back-grinding, in order to reduce the bumps and dips and round the corners, thereby improving the coverage of films.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a cross-sectional view showing a manufacturing method of a semiconductor device according an embodiment of this invention.

[Fig. 2]

Fig. 2 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

[Fig. 3]

Fig. 3 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

[Fig. 4]

Fig. 4 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

[Fig. 5]

Fig. 5 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

[Fig. 6]

Fig. 6 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

[Fig. 7]

Fig. 7 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

[Fig. 8]

Fig. 8 is a cross-sectional view showing the manufacturing method of the semiconductor device according the embodiment of this invention.

[Fig. 9]

Fig. 9 is oblique perspective views showing a manufacturing method of a semiconductor device according to a conventional art.

[Fig. 10]

Fig. 10 is a cross-sectional view showing the manufacturing method of the semiconductor device according to the conventional art.

[Document Name] Abstract
[Summary]
[Subject] Yield and reliability of a BGA type semiconductor device are improved.
[Solving Means] A glass substrate 4 which works as a supporting plate is bonded through an adhesive 5 to a surface of a semiconductor wafer 1a on which first wirings 3 are formed. Thickness of the semiconductor wafer 1a is reduced by back-grinding the semiconductor wafer on a surface of the semiconductor wafer which is opposite to the surface to which the glass substrate 4 is bonded. The semiconductor wafer 1a is wet-etched to remove bumps and dips on the surface of the semiconductor wafer 1a caused by scratches during the back-grinding. Then the surface of the semiconductor wafer opposite to the surface to which the glass substrate 4 is bonded is etched to form a tapered groove along border lines. The semiconductor wafer is wet-etched to reduce bumps and dips caused by the etching and round a corner of the groove. The wet-etching improves coverage of an insulation film, wiring and a protection film formed after the etching and enhances yield and reliability of the semiconductor device.
[Selected Figure] Fig. 8

FIG.1

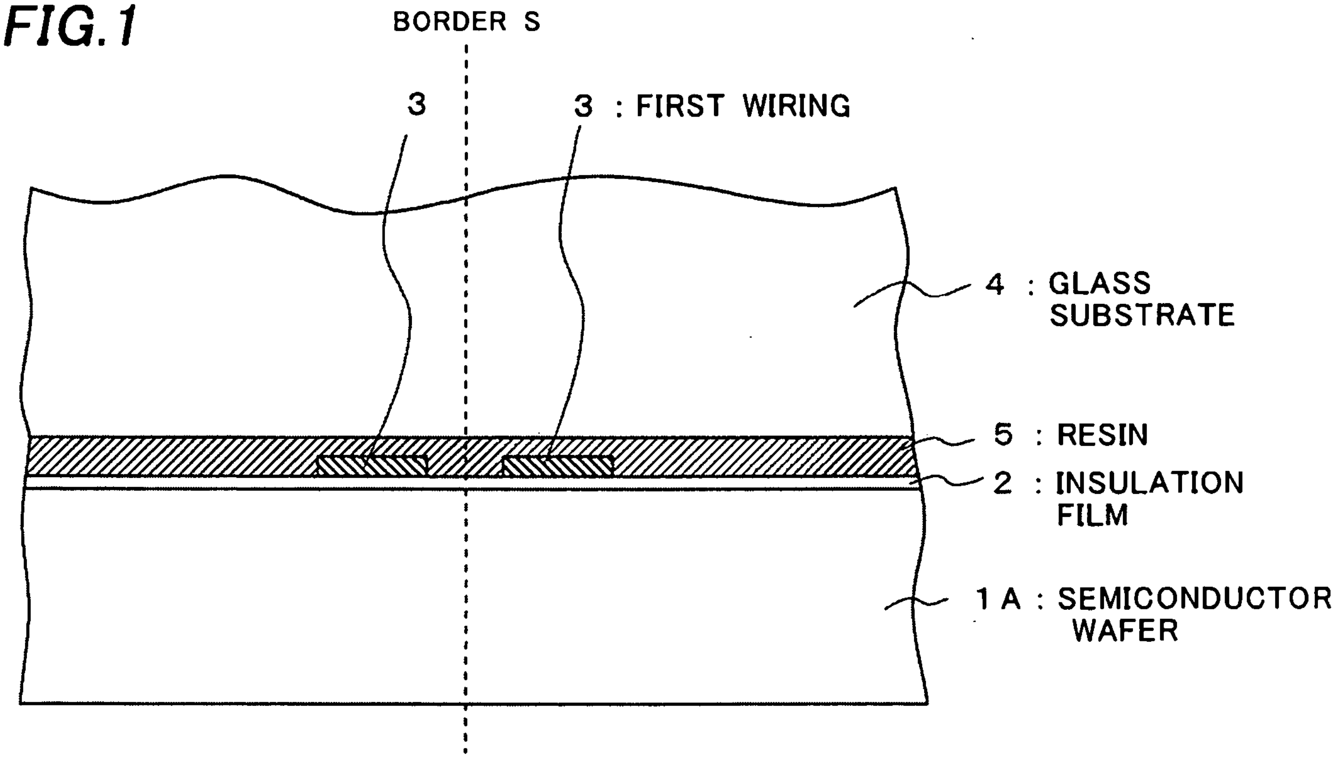

BORDER S
3
3 : FIRST WIRING
4 : GLASS SUBSTRATE
5 : RESIN
2 : INSULATION FILM
1 A : SEMICONDUCTOR WAFER

FIG.2

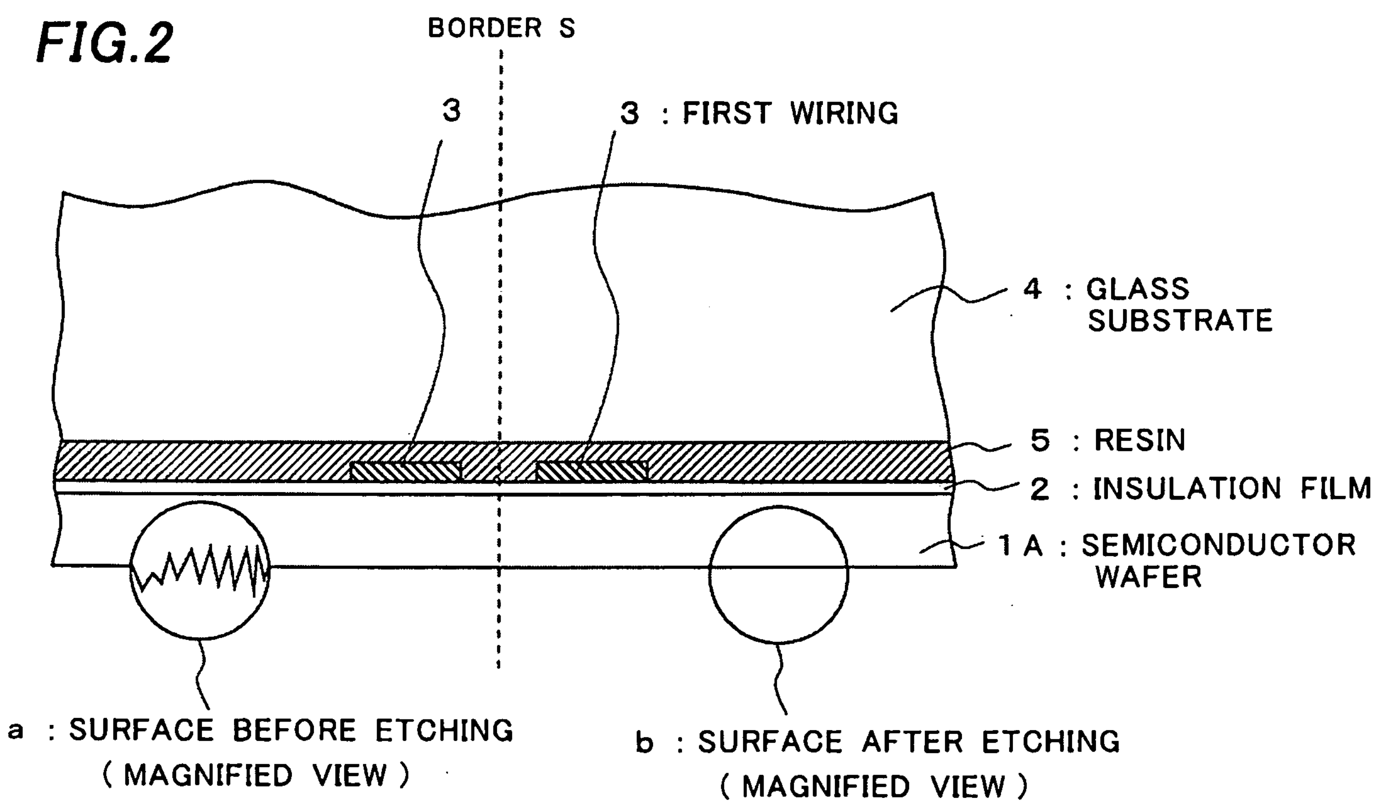

BORDER S
3
3 : FIRST WIRING
4 : GLASS SUBSTRATE
5 : RESIN
2 : INSULATION FILM
1 A : SEMICONDUCTOR WAFER
a : SURFACE BEFORE ETCHING
( MAGNIFIED VIEW )
b : SURFACE AFTER ETCHING
( MAGNIFIED VIEW )

FIG.3

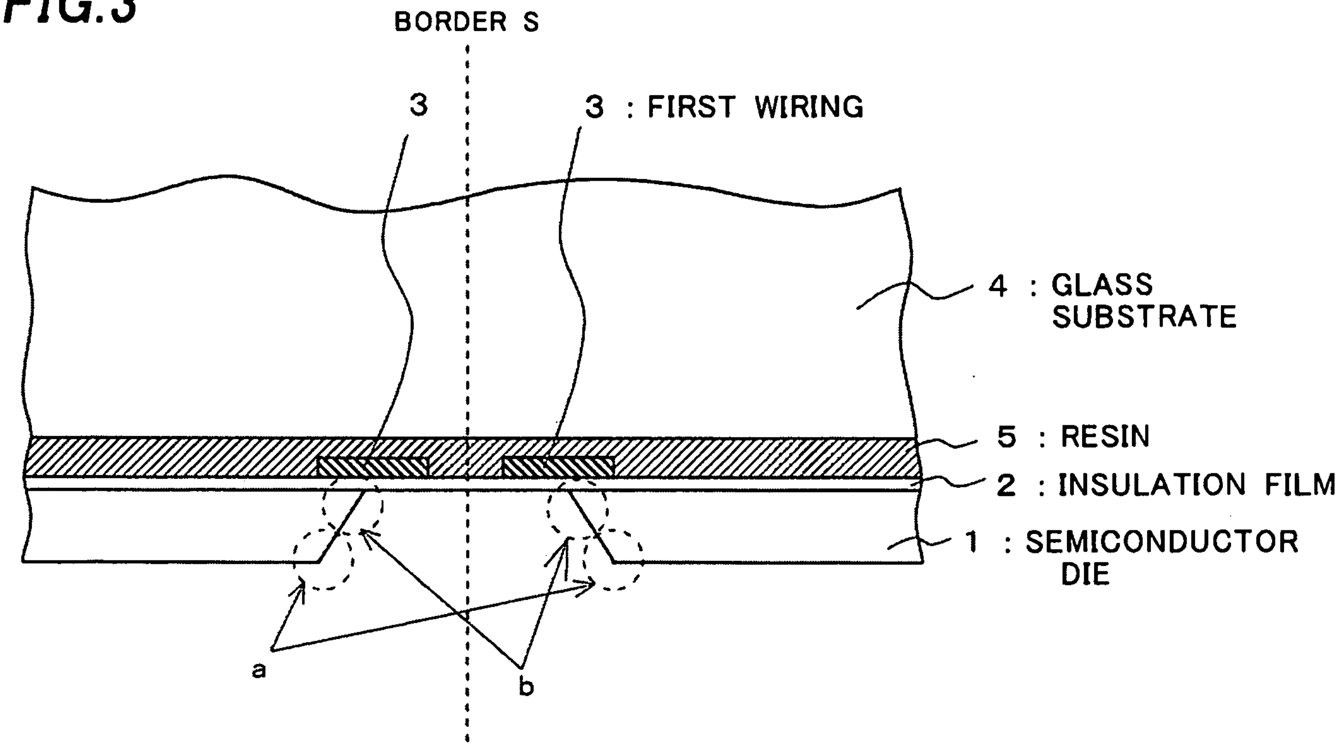

BORDER S
3
3 : FIRST WIRING
4 : GLASS SUBSTRATE
5 : RESIN
2 : INSULATION FILM
1 : SEMICONDUCTOR DIE
a
b

FIG.4

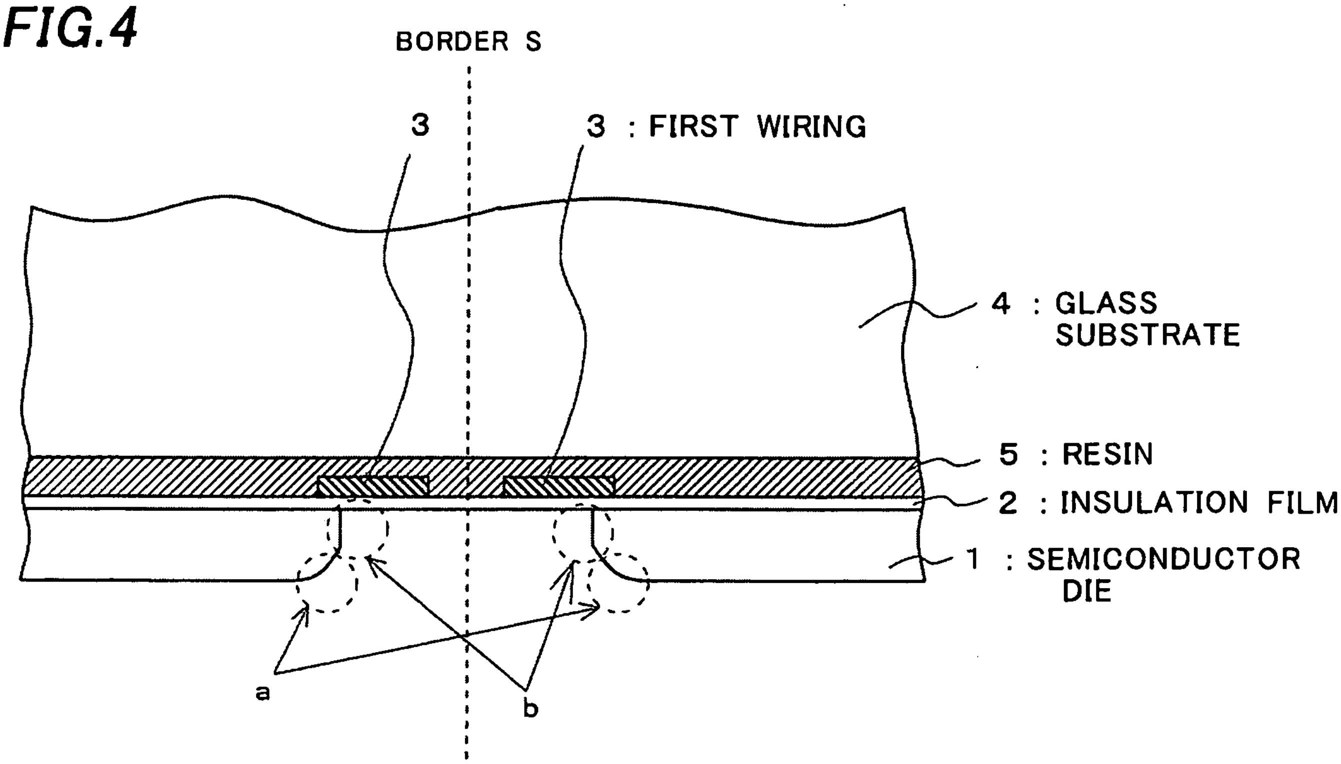

BORDER S
3
3 : FIRST WIRING
4 : GLASS SUBSTRATE
5 : RESIN
2 : INSULATION FILM
1 : SEMICONDUCTOR DIE
a
b

FIG.5

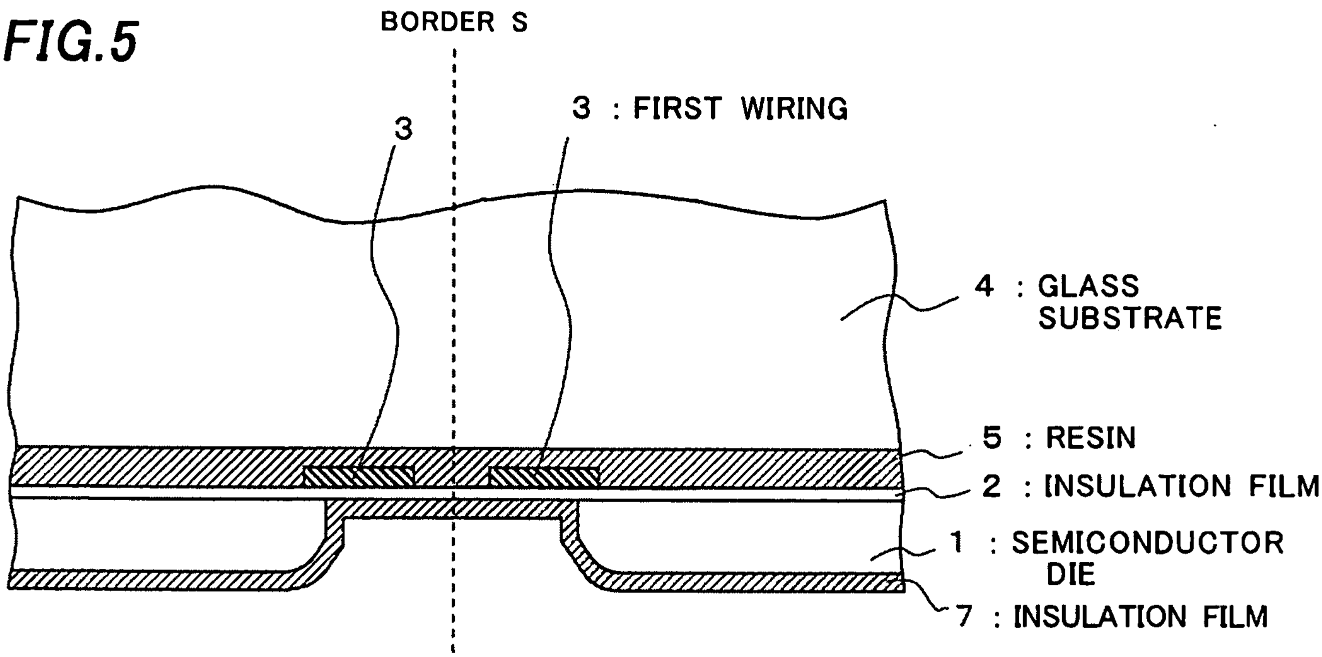

BORDER S
3
3 : FIRST WIRING
4 : GLASS SUBSTRATE
5 : RESIN
2 : INSULATION FILM
1 : SEMICONDUCTOR DIE
7 : INSULATION FILM

FIG.6

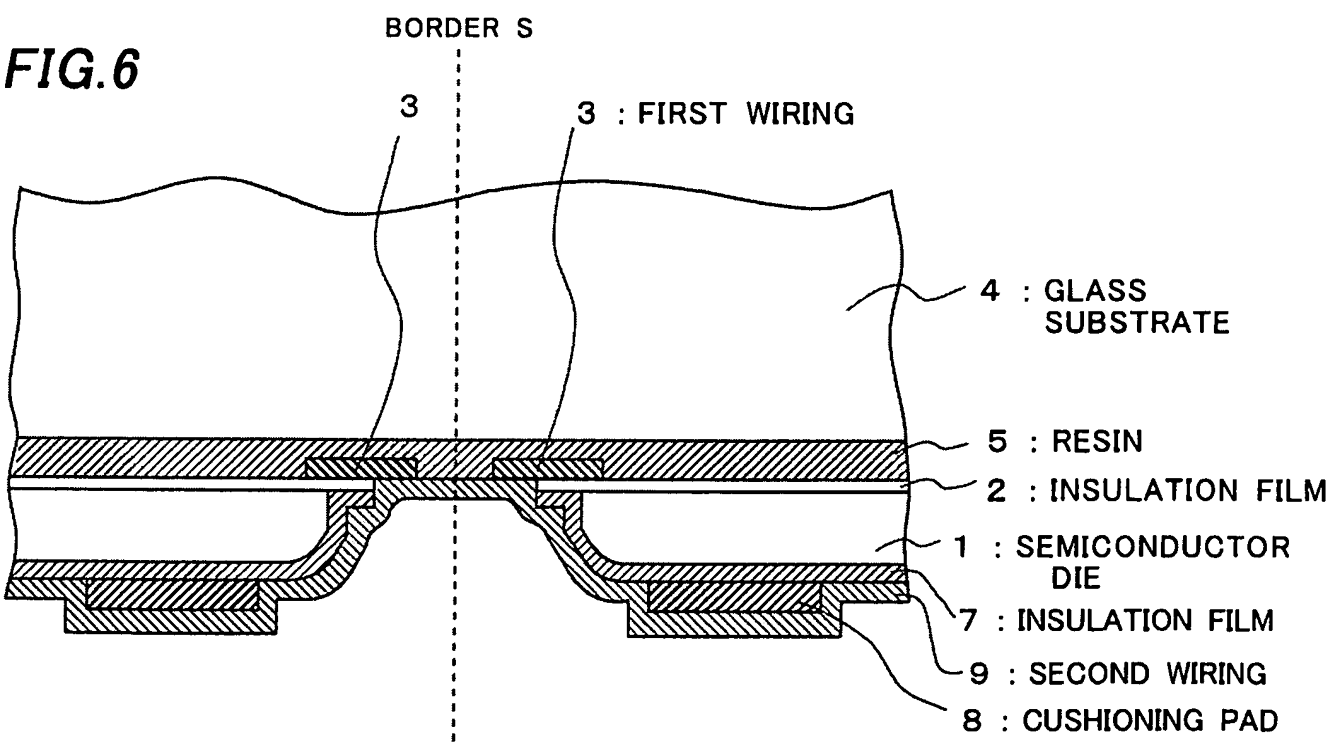

BORDER S
3
3 : FIRST WIRING
4 : GLASS SUBSTRATE
5 : RESIN
2 : INSULATION FILM
1 : SEMICONDUCTOR DIE
7 : INSULATION FILM
9 : SECOND WIRING
8 : CUSHIONING PAD

FIG.7

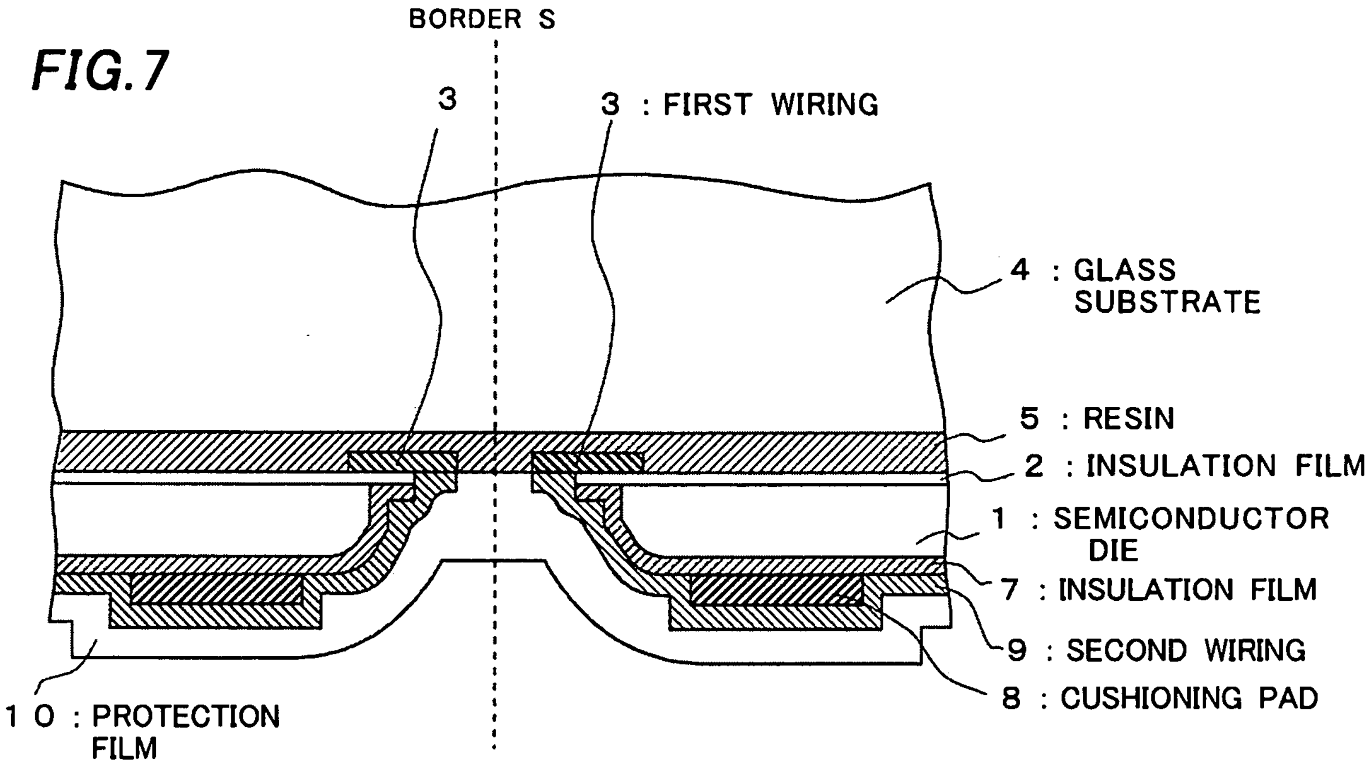

BORDER S
3
3 : FIRST WIRING
4 : GLASS SUBSTRATE
5 : RESIN
2 : INSULATION FILM
1 : SEMICONDUCTOR DIE
7 : INSULATION FILM
9 : SECOND WIRING
8 : CUSHIONING PAD
1 0 : PROTECTION FILM

FIG.8

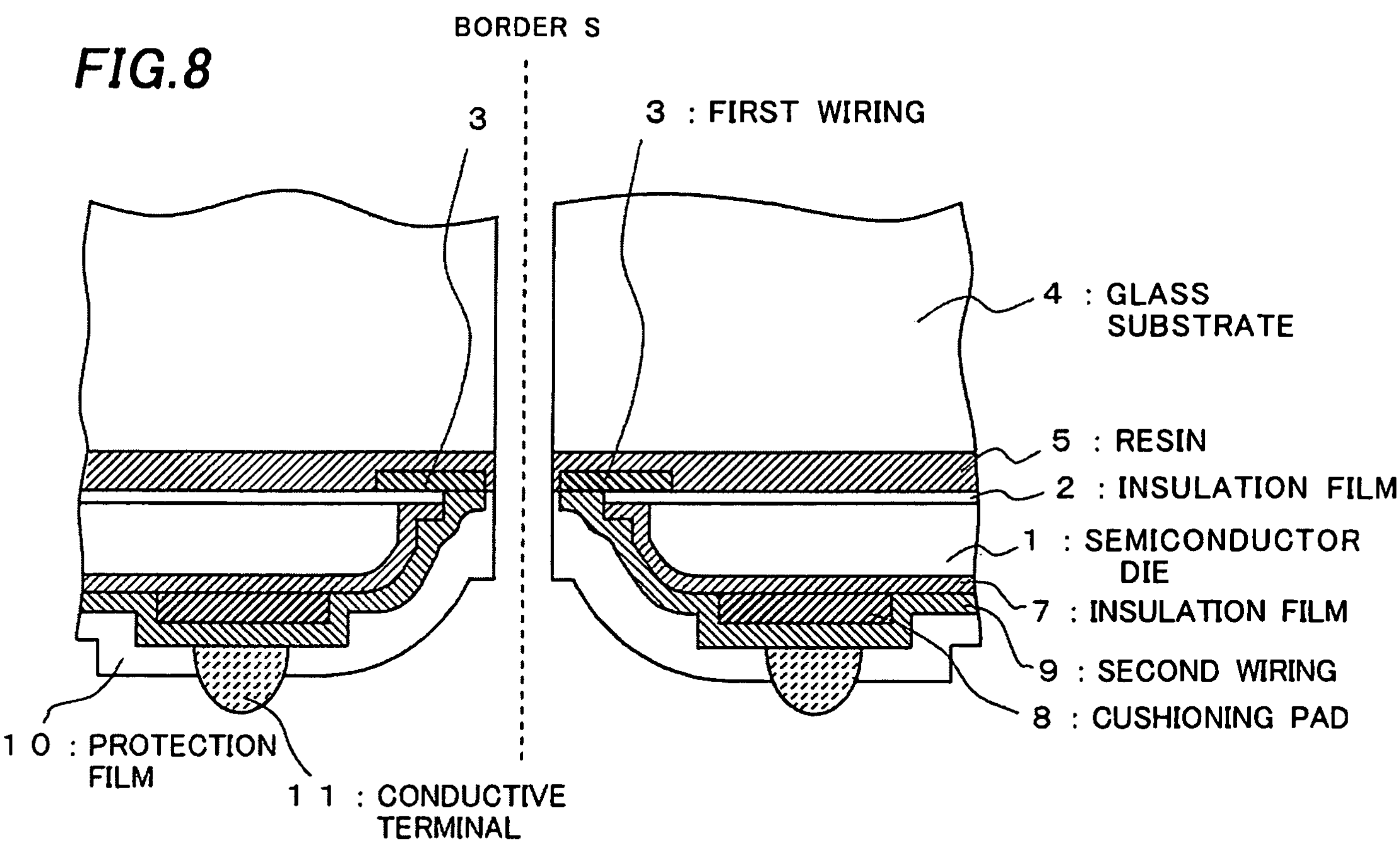
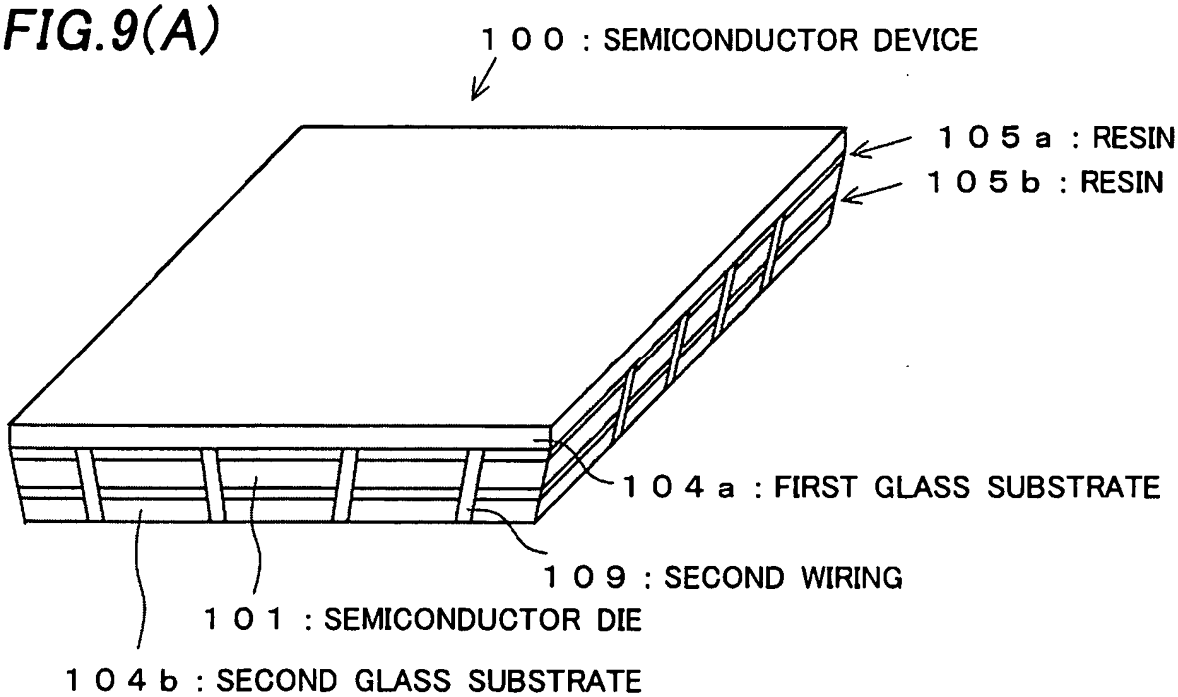
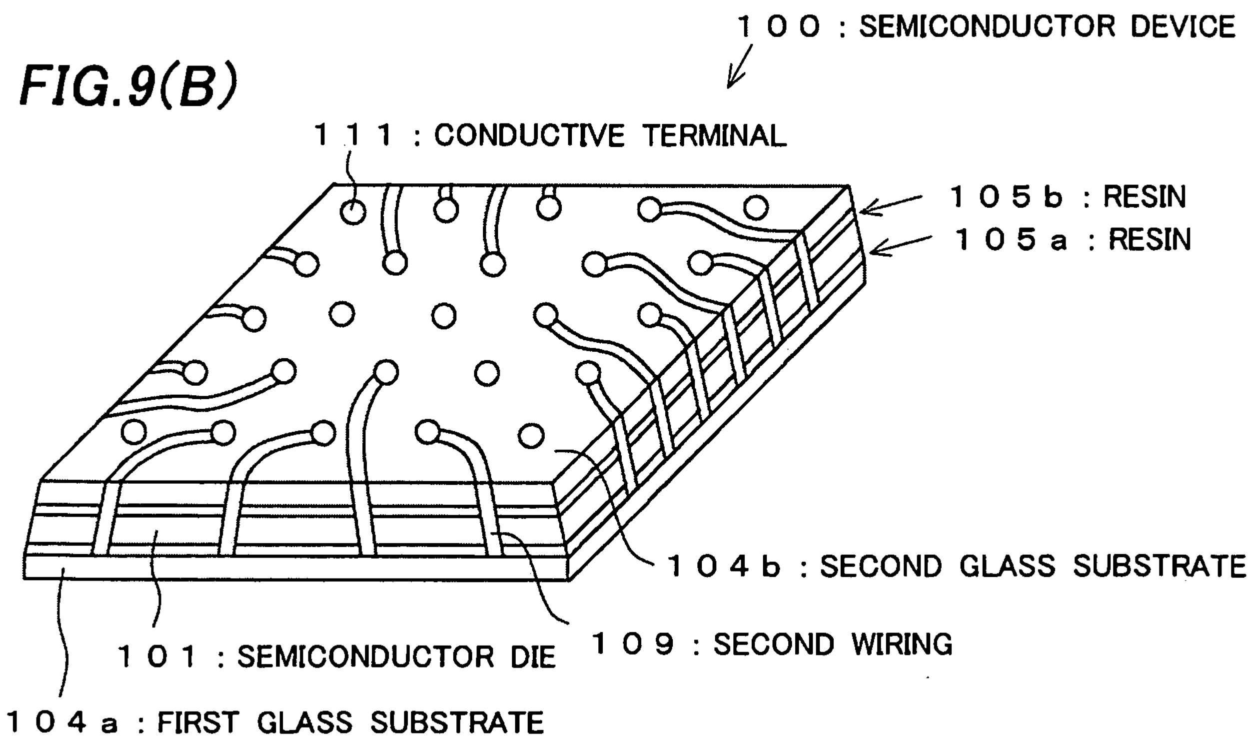

BORDER S
3
3 : FIRST WIRING
4 : GLASS SUBSTRATE
5 : RESIN
2 : INSULATION FILM
1 : SEMICONDUCTOR DIE
7 : INSULATION FILM
9 : SECOND WIRING
8 : CUSHIONING PAD
1 0 : PROTECTION FILM
1 1 : CONDUCTIVE TERMINAL

FIG.9(A)



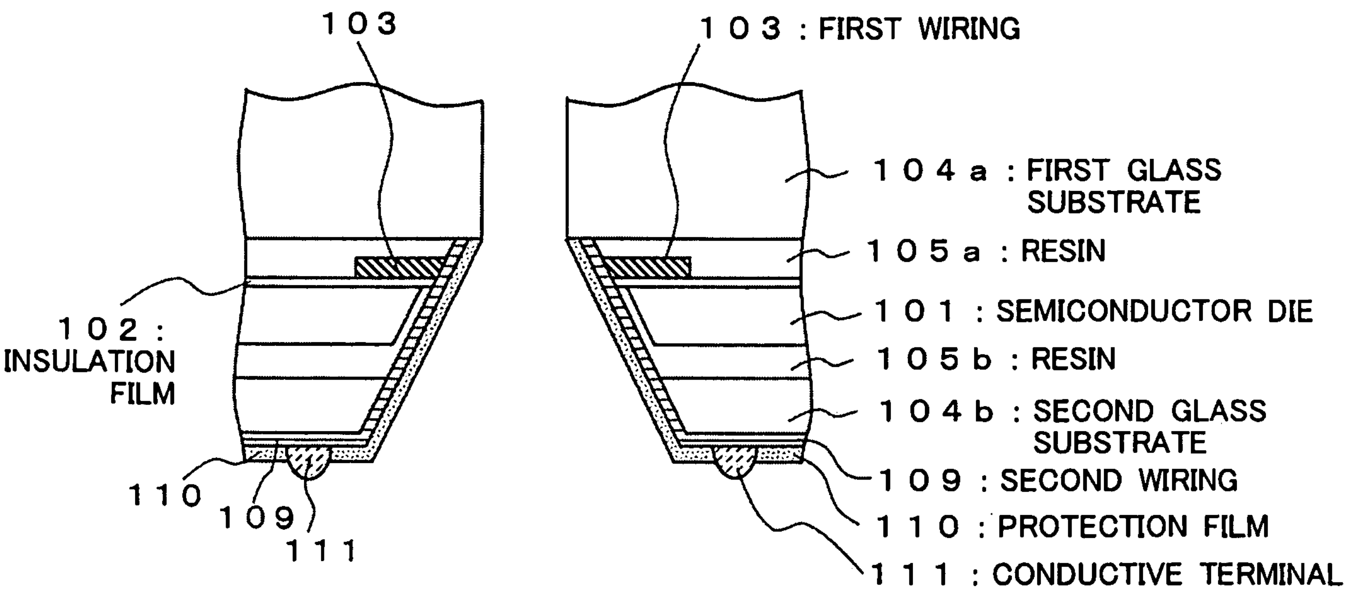
1 0 0 : SEMICONDUCTOR DEVICE
1 0 5 a : RESIN
1 0 5 b : RESIN
1 0 4 a : FIRST GLASS SUBSTRATE
1 0 9 : SECOND WIRING
1 0 1 : SEMICONDUCTOR DIE
1 0 4 b : SECOND GLASS SUBSTRATE


FIG.9(B)



1 0 0 : SEMICONDUCTOR DEVICE
1 1 1 : CONDUCTIVE TERMINAL
1 0 5 b : RESIN
1 0 5 a : RESIN
1 0 4 b : SECOND GLASS SUBSTRATE
1 0 9 : SECOND WIRING
1 0 1 : SEMICONDUCTOR DIE
1 0 4 a : FIRST GLASS SUBSTRATE

*FIG.10*


103
102 : INSULATION FILM
110
109
111
103 : FIRST WIRING
104a : FIRST GLASS SUBSTRATE
105a : RESIN
101 : SEMICONDUCTOR DIE
105b : RESIN
104b : SECOND GLASS SUBSTRATE
109 : SECOND WIRING
110 : PROTECTION FILM
111 : CONDUCTIVE TERMINAL